Using the Logic Design Course as a Dress Rehearsal for the Major Design Experience

Paul Crilly, Grant C. Wyman
Department of Engineering, Electrical Engineering
U.S. Coast Guard Academy, New London, CT 06320
Paul B. Crilly@uscga.edu

Abstract - *We describe a sophomore level course that is foremost a comprehensive treatment of logic design, a mandatory topic in many electrical and computer engineering curriculums, but almost equally important, because of the open ended design content, this course serves as the dress rehearsal for what students will encounter in their required senior capstone project. Course outcomes and goals include the usual engineering technical topics such as Boolean algebra, logic design, finite automata, discrete math, modern engineering tools, and solving engineering problems. We also cover and assess those outcomes that are not covered in most of the other engineering courses which include open ended design, multidisciplinary teams, and effective communication. This early assessment in these nontechnical outcomes, allows us earlier intervention for program improvement. Having conducted this course over a period of over six years, we have found that our approach has helped us achieve a marked improvement in both our student outcomes, and the quality of our capstone projects*.

Keywords- Capstone projects, engineering design education, assessment, logic design, accreditation.

I. Introduction

According to the EAC ABET criterion, an accredited engineering program requires a "… major design experience based on the knowledge and skills acquired in earlier course work and incorporating appropriate engineering standards and multiple realistic constraints."[1] In many schools, this criterion is satisfied by the one or two semester senior level "capstone course." Furthermore, the capstone course is the vehicle used to assess several of the ABET *a-k* outcomes such as design, effective communication, engineering tools, and multidisciplinary, etc. which are not easily assessed in most of the traditional specific subject engineering-science courses. Thus Program Chairs heavily rely on the capstone for much of this important assessment information. This is a heavy burden to place on one course – a single snapshot of student performance. Thus if a student has a shortcoming, but improves later on, there may be little opportunity to demonstrate improvement or document that this particular outcome has been met. Finally, engineering students are by nature creative, and thus there should be more than one opportunity to practice design. Similarly, there should be more opportunity to perfect their communication skills, and otherwise enable them to become more proficient in all the other *a-k* student outcomes. In this paper, we discuss how we use our sophomore level logic design course as a dress-rehearsal for the senior level capstone design experience as well as acquire early direct assessment information. Preliminary assessment data has shown that this mini-capstone experience enables our students to better achieve the stated student outcomes in the senior capstone course.

The literature is replete regarding the topic of integrating design into the engineering curriculum. Catalano [2], Baily [3], present an overall view of design education including the multidisciplinary design, the challenges of offering real-world projects versus "made up projects" devised by faculty [4] and learning engineering design in conjunction with entrepreneurial pursuits [5]. While most if not many capstone projects are in the senior year, some programs [6-8] desire to push engineering design down so it occurs earlier in the curriculum and thereby provide additional opportunities to develop a student's ability to do engineering design.

II. Course Coverage

The overriding learning objective of any logic design course is that the student will be a proficient logic design engineer. That is, if a solution requires a logic circuit, a student can take the specifications and turn them into a working prototype circuit using the appropriate technology. Therefore, in the first two thirds of our course we cover classical combinational and sequential logic theory and design, as well as number systems. We augment the theory using appropriate lab exercises that include mixed signal, data transfer from a computer system via a graphical user interface (GUI) and electromechanical systems. The last third of the course is the mini-capstone project and is designed to integrate all that they have learned.

Logic theory and design topics: The textbook for the course is F. Vahid's book, *Digital Design, With RTL Design, VHDL and Verilog*[9]. We cover the following topics:

[1] ABET EAC Criteria Section 5.

Number systems, Boolean algebra, truth tables, logic synthesis, logic and state minimization, high order logic functions such as multiplexors, arithmetic units, logic technologies, and finite state machines. Instead of implementing a processor via the conventional Algorithmic State Machine (ASM) approach, we take Vahid's approach and use Register Transfer Logic (RTL) where the processor has two subsystems – the *controller*, which is a conventional finite state machine (FSM), and the *data path*, which contains all the computation logic and is controlled by the FSM. Students also learn about the various logic technologies such as PLDs, ROMS, RAMS, and FPGAs. We also provide a brief treatment of the hardware description language Verilog.

Logic theory projects: There are two laboratory projects used to augment and reinforce the lecture material. The first one is where students design a bidirectional data path where either data from an analog-to-digital converter (ADC) is inputted into computer, or we can choose to have computer generated numbers outputted to a digital-to-analog converter (DAC). The data transfers and direction are initiated by the computer's GUI. The block diagram for this system is shown in Figure 1. The ADC's input is 0 to 5 volts from a potentiometer, and the output from the DAC is a voltmeter. The GUI sends out an address corresponding to the data direction which is decoded by the hardware. This project is done in stages over a period of six weeks. Students learn the practical aspects of using discrete logic gates, logic decoders, mixed signal components, registers, and computer interfacing, and of course troubleshooting.

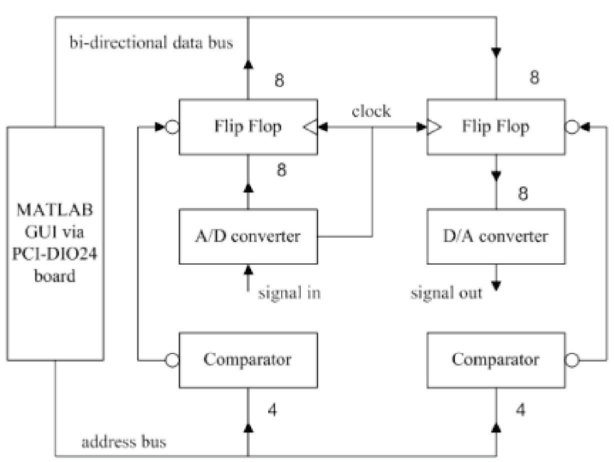

Figure 1. Block diagram of bidirectional data bus.

The second project is to implement a FSM controller via an FPGA that emulates a combinational lock. Here the students have to define and then implement a FSM controller. In doing so they learn the various design tools such as Schematic Capture, Verilog, NI Multisim™ and the usual practical design items such as clocking, set up times, switch debounce, and metastability. This is not a simple task since there are a host of practical issues associated with an electromechanical combinational lock and using a FSM controller that runs on 10 MHz clock. In other words, students find out that implementing FSM from a paper design using real hardware is not trivial and there are many subtleties in getting a practical FSM with external inputs to behave as expected and meet the expected design goals.

Capstone Project: During the last third of the semester, the class is then divided into two-person teams where they choose or initiate an open ended design project that mimics our senior design experience except at a lower level and focuses on digital systems. Typically this also involves electromechanical and mixed signal design where they have to also apply what they learned in previous courses such as circuits, electronics, programing, and signal processing. Students spend 100% of the course time engaged in all aspects of the project design including periodic project reviews conducted with their advisor and practice presentations with their classmates. At the end of the semester, they present their project alongside the seniors at our senior design symposium. They also do a heavily critiqued written paper. The executive level symposium provides a means for the sophomore students to develop their written and oral communication skills and receive valuable feedback from the faculty, students and our external stakeholders. As a result of this "dress rehearsal" the students do a better job of achieving the student outcomes in their senior capstone course.

The following are projects we have done in the past: (a) Elevator control circuit, (b) TTY radio transmitter, (c) M & M candy dispenser, (d) Frequency counter, (e) Hi-lo game, (f) Whack a Mole game, (g) Clothes washing machine controller, (h) Change counter, (i) Rock, paper scissors, lizard, Spock contest, (j) Ship rudder control, and (k) Luggage lock. These projects involved mixed signal circuits, and external logic. Most of the projects also involve logic hardware controlling external motors or solenoids. See Figures 2a-e for illustrations of student projects. As readily observed, the projects consisted of logic breadboards, external mechanical hardware, a computer and sometimes an FPGA development board. Typically the computer provides a GUI input to initiate data transfers with the external hardware.

III. Assessment

This course emulates the four year undergraduate experience in that the first two thirds covers basic engineering science, and then culminates in a comprehensive capstone experience that

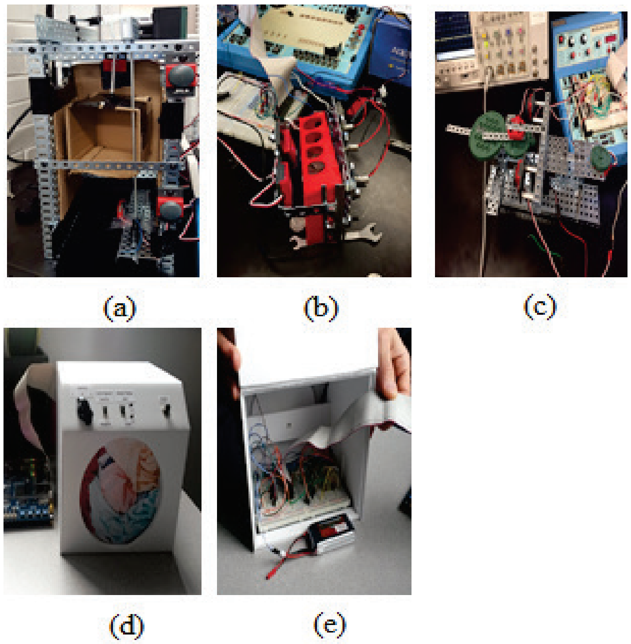

Figure 2. Digital capstone projects. (a) Elevator, (b) Change counter, (c) Ship rudder, (d,e) Washing machine.

ties together what they earlier learned as well as what they learned in other courses. Like the senior capstone course, several ABET outcomes are assessed with the results used to improve the program. Assessed student outcomes using the *(a)* to *(k)* ABET identifiers include the following: *(c)* An ability to design a system to meet desired needs within realistic constraints, *(d)* An ability to function on multidisciplinary teams, *(e)* An ability to function to identify, formulate and solve engineering problems, *(g)*, An ability to communicate effectively, *(k)* An ability to use techniques, skills and modern engineering tools necessary for engineering practice, and a basic knowledge of discrete math. As a result of this "dress rehearsal," preliminary assessment data indicates an improvement in several student outcomes for the senior capstone course. Furthermore, alumni feedback has indicated that the lessons learned in this course were invaluable for their engineering careers.

IV. Conclusion

In this paper we have presented a means to ensure better attainment of student outcomes. The capstone design dress rehearsal is done in the sophomore year has greatly contributed to the marked improvement in student outcomes such as written and oral communication. The clear evidence of this improvement is the increased attendance by our stakeholders at the senior capstone presentations. Many if not most of these stakeholders hire our students upon graduation. Furthermore, because the logic design course is relatively comprehensive, we can provide more challenging projects for the senior capstone course.

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